

A3949

DMOS full-bridge motor driver IC

New from Allegro MicroSystems Europe, the A3949 is a DMOS full-bridge motor driver integrated circuit designed for the PWM (pulse-width-modulated) control of DC motors.

The new device is capable of peak output currents of up to ± 2.8 A and operating voltages of up to 36 V, and has low 'on' resistance outputs: typically 0.68 ohm for the source driver and 0.576 ohm for the sink driver.

'Phase' and 'enable' input terminals are provided for controlling the speed and direction of the motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to reduce power dissipation during PWM operation.

A 'sleep' mode, implemented via a logic 'low' on a dedicated input terminal, is provided to minimise power consumption when the A3949 is not in use. This disables much of the internal circuitry, including the low-side gate supply and the charge pump.

A braking function is implemented by driving the device in slow decay mode via the 'mode' pin, and applying an 'enable chop' command. Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts out the motor-generated back EMF.

Internal circuit protection includes thermal shutdown with hysteresis, undervoltage monitoring of load supply and charge-pump voltages, and crossover current protection.

The A3949 is supplied in a choice of two power packages, a 16-lead plastic SOIC with a copper batwing tab (suffix LB), and a low-profile (1.1 mm) 16-lead TSSOP (suffix LP) with exposed power tab. Operating temperature range is -20°C to $+85^{\circ}\text{C}$.
